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This report covers the technical progress of the program over the six-month period, February 15, 1979 to August 15, 1979. Its organization corresponds to that of the contract proposal with sections devoted to Thermal Oxidation, Ion Implantation, Chemical Vapor Deposition of Silicon, Materials Analysis and Interface Physics, and Complete Process and Device Simulation. Each section contains a description of progress made, including difficulties encountered, results obtained with their supporting data, and brief plans for the future.

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SEMI-ANNUAL TECHNICAL STATUS REPORT

February 15, 1979 - August 15, 1979

MODELS OF FABRICATION PROCESSES, DEVICES, CIRCUITS, AND SYSTEMS FOR COMPUTER-AIDED DESIGN OF VLSI

Contract No. MDA 903-79-C-0257

Introduction

This report covers the technical progress of the program over the six-month period, February 15, 1979 to August 15, 1979. Its organization corresponds to that of the contract proposal with sections devoted to Thermal Oxidation, Ion Implantation, Chemical Vapor Depostion of Silicon, Materials Analysis and Interface Physics, and Complete Process and Device Simulation. Each section contains a description of progress made, including difficulties encountered, results obtained with their supporting data, and brief plans for the future.

THERMAL OXIDATION

J. Plummer, B. Deal, W. Tiller, R. Razouk, C. Ho, L. Lie, H. Massoud

A. High Pressure Oxidation System

Gasonics' High Pressure Oxidation (Hipox) System was installed. Preliminary testing followed the installation of pumps for boosting the in-house liquid sources of O_2, N_2, and H_2 to the required 1000-1200 psi pressure. One of the most important instruments added to the system were mass flowmeters used to monitor more accurately the gas flow rates and thus the oxidant partial pressure.

A start-up contract was purchased from Applied Materials to check the system operation. A number of runs were carried out. Worst case non-uniformity across a wafer was ±3.8%, wafer to wafer oxide thickness variations were less than ±2.2%, and run to run average was 1.04 μm ±1.6% for a 45 min oxidation of (100) Si in a steam ambient at 25 atm, 920°C.

Two alternate pressurization procedures to be used as standard routines in the gathering of kinetic data were investigated:

(1) Pressurization in nitrogen followed by oxidation in steam. The main questions to be answered dealt with possible N_2 reaction with silicon at high pressure, and the transition time required to change the N_2 ambient to a steam ambient.

(2) Pressurization and oxidation in steam. Questions were raised about the reproducibility of pressurization rate.

In the first case preliminary Auger examination of a bare silicon wafer annealed at 25 atm, 1000°C for 20 min in N_2 showed the formation of 60 Å of SiO_2 due to residual O_2 in the nitrogen, and revealed the presence of N_2 at the Si-SiO_2 interface which could retard subsequent oxide growth. This combined with the lack of a direct method to measure or detect the reproducibility of the transition time led us to abandon this oxidation scheme.

In the second case, the reprodicibility of the pressurization stage was tested by installing a strip chart recorder, HP7101B, to record the pressure of the system during the entire oxidation cycle. Results indicated very good reproducibility in pressurization rate. The second procedure which consists of pressurization and oxidation in steam was therefore adopted as the standard in gathering of kinetic data.

Preliminary kinetic analysis on oxide growth under pressure using data available from T. Thompson of Applied Materials were carried out.

Initial runs for high pressure oxide growth characterization were carried out at 1 atm in steam (control runs), and in dry O_2 as well as at 10 atm in steam for a temperature range of 800°C to 1000°C.

B. Effect of Cooling Procedures on Oxide Charges

It was observed that subtle variations in the cooling procedure can have substantial effects on the resulting oxide charges, particularly in the case of samples cooled in the oxidizing ambient. Results are shown here for wafers oxidized in dry O_2 at 1200°C and cooled in the oxidizing ambient following a fast pull (<3 sec). Differences between the runs centered around the placement of the wafers in the boat (i.e. upright in the boat or flat on the boat) and the presence or absence of an elephant in which the wafers are cooled. The results are shown in Fig. 1 where the effects on N_f are illustrated. Minimum N_f values are obtained with the wafers upright and interacting with the ambient (open tube), while maximum values are obtained with the wafers flat on boat (longer cool time) and enclosed in the elephant. The reproducibility of the N_f triangle from this experiment and others is found to be dependent on a quick cool. In situations where there is slower cooling, use of a closed elephant, or during the processing of a large number of wafers, the resulting oxide charge levels can be quite different.

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C. N_f Determination for Thin Oxides

Experiments were carried out to verify presently used values of metal-semiconductor work functions ϕ_{MS} for Al-Cu-Si field plates on p- and n-type silicon substrates. A second purpose for the experiments

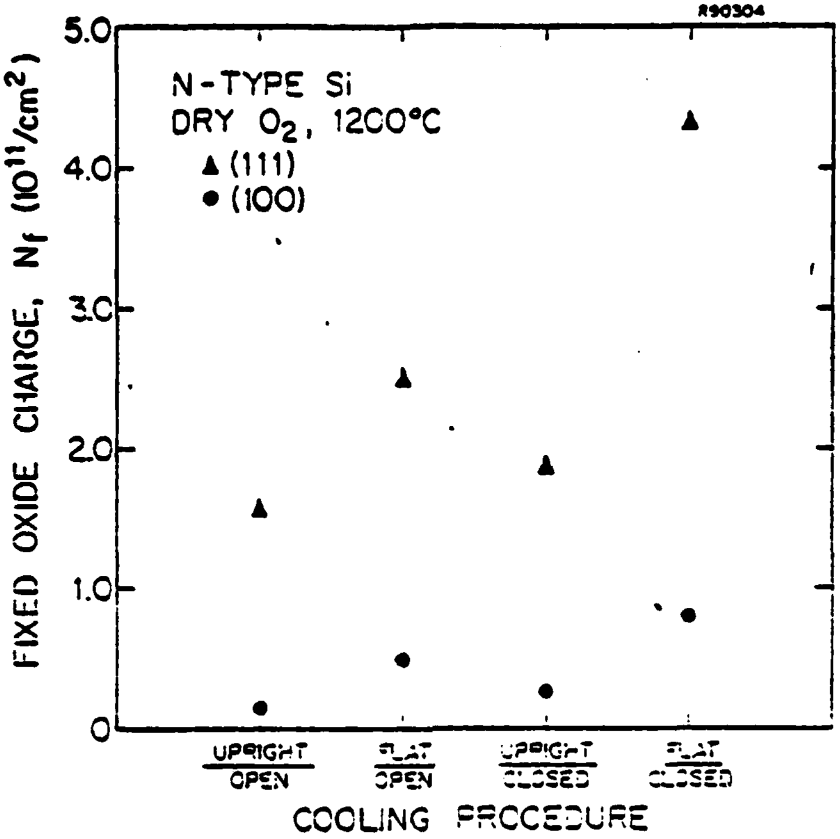

Fig. 1 Dependence of fixed oxide charge density on the exact cooling procedure. Upright or flat indicates whether the wafers are upright in the boat or flat and touching the boat. Open or closed refers to open tube end or closed end (pull into an elephant).

was to reaffirm that the oxide fixed charge N_f is independent of oxide thickness.

P- and n-type silicon wafers, (100) and (111), 4-9 Ω-cm were oxidized in dry O_2 at 1000°C for various times and cooled in nitrogen (N_2 SP). Results obtained indicate that N_f is indeed constant for the oxide growth conditions described. ϕ_{MS} values of -0.1 and -0.7 volts were obtained for Al-Cu-Si fieldplates on n- and p-type silicon substrates, respectively. The updated ϕ_{MS} values will be used in all future oxide fixed charge measurements. Some variation was observed between (100) and (111) work-function differences and will be investigated further.

D. Effect of Wafer Orientation on Oxide Charge Densities

As part of our continuing investigations of oxide charges, differences resulting from a slice misalignment were investigated. This was carried out primarily because most p-type (111) material available commercially has a slice misalignment of 4° from (111) toward (110) parallel to the flat. The effect of this misalignment on oxide charges was investigated and a 2-13% variation in fixed oxide charge and interface state density observed with the (111) +4° silicon yeilding lower oxide charges as expected.

E. Physcal Modeling of the Oxidation Process

Both qualitative and quantitative analyses of the effect of an interface field on solute redistribution during a phase transformation at constant velocity have been conducted. The interface field may be a stress field, either electrical field or other type of field, and of short range or long range. A rigorous mathematical analysis of the steady state distribution for a two-phase system transforming at constant velocity and with an interface distribution coefficient, k_i , and a net interface distribution coefficient, k_i^* , have been used to describe the equilibrium and kinetic field effects while k_i^* has been evaluated as a function of k_i and V for a variety of numerical cases. One expects k_i^* to be orientation dependent since it depends on the magnitude and extent of the interface field, which is expected to be orientation dependent, and also upon the ratio of the solute diffusion coefficient, D , to the interface velocity, V.

Extensive attempts to obtain a rigorous initial transient distribution for the solute redistribution process in the presence of an exponential interface field have not yet been completely successful. This is essential for the application of such concepts to the thermal oxidation of Si since the constant velocity regime is short lived in that case. However, an approximate theoretical model for phosphorus redistribution during thermal oxidation for an interface field, which is a square well potential of some width d and depth U at the interface and is zero at larger distances, has been developed. Theory predicts that the interface region will be 90% saturated with P after 90 minutes of oxidation at 900°C and after 420 minutes at 800°C. At earlier times (10 minutes at 900°C) the theory predicts a smaller pile-up and, just outside of the interface on the Si side, a depletion of P. All of these results were confirmed by Auger concentration profile measurements. Within the limits set be the Auger technique, which tends to broaden the peak of the concentration profile, estimates of the P pile-up width are $25\ \text{Å} < d < 47\ \text{Å}$. The surface segregation of phosphorus, $m = \exp(Q/kT)$, is experimentally found to be defined by the limits $0.22\ \text{eV} < Q < 0.52\ \text{eV}$ and $9 < m < 170$ while the limits on U are $0.2\ \text{eV} < U < 5.2\ \text{eV}$.

ION IMPLANTATION

G. Gronner, L. Christel, J. Gibbons, C. Ho, S. Mylroie, J. Plummer

A. Boltzmann Transport Modeling of Implanted Ion Range Statistics

As reported earlier, by March 1979 a computer program which calculates the concentration profiles of ions implanted into multilayered targets by integrating the Boltzmann equation was written and in fair working order. In the months of March and April, this program was tested by calculating profiles for common ions (B, P, As) and comparing the results with published experimental data. [1,2].

It was found that the caluclated boron profiles were in error by quite a bit; they showed much less skewing than experimental profiles. This led to a search for errors and indeed a bug was found and corrected. The corrected program produced results which agree with experimental data to about the same accuracy as LSS moment calculations [3] (about 10-20%). This level of accuracy seems to hold over a wide range of ion-target combinations.

The main drawback of the program at this point was its very long execution time - about 5 minutes of CPU on the IBM 370/168. There is hope however that the algorithms involved can be streamlined and simplified.

Through the summer months, the Boltzmann program was set aside and work was done on the simulation of ion channeling in crystalline solids. The [110] direction of silicon was modeled as six string potentials arranged in a near hexagonal configuration. The trajectories of individual particles were then studied as a function of position of entry down the channel.

Experimentally it is observed that when ions are implanted at e.g. 8° from a high symmetry direction, the concentration profiles show an exponential tail. It was our hope that the simulation results might give a clue to how these occur. It was found that this behavior is most probably a geometrical effect - i.e. due to the fact that the two dimensional cross section of the channel favors the probability for ions to enter off center, and not to enter straight down the channel on axis. Unfortunately the results do not seem to be particularly useful at the present time and work on this has been suspended for the moment.

Starting in August, work on the Boltzmann program was resumed. The job of incorporating recoils into the calculation was begun and attempts to simplify the code were made. The progress on this looks very good and will be reported in the annual report.

B. Implant Damage Effects on Thin Oxides

The substrate itself can be severely damaged by implantation. An initially crystalline substrate may be driven amorphous or large densities of vacancy-interstitial point defect pairs created. With the developing view of the central role of point defects in most high temperature processes involved in device fabrication, such implant damage may substantially influence those other processes both in the implanted region and in adjacent areas of the device wafer.

An attempt was made to determine the scope and magnitude of implant damage effects specifically on silicon oxidation kinetics and oxide charges in the thin oxide regime. Purely-implant damage introduced by Si^+ self-implants in samples driven amorphous was found to substantially retard the oxidation rate in the thin oxide regime under some ambient and temperature conditions. Damaged samples that were first thermally annealed before oxidation did not exhibit the altered oxidation rates.

Impurity effects were added to the damage effects via implantation of both relatively inert impurities such as Ar, F, and Cl and electrically active dopants such as B, P, and As. Both retardation and enhancement of oxidation rates were observed, in agreement with the few reports found in the literature. As also observed in the literature, however, reproducibility was poor and insufficient for quantitative modeling, emphasizing the transient nature of the multiple mechanisms likely participating. The net oxidation rate likely results from the intrinsic interface oxidation mechanism and the damage annealing/solidphase epitaxial regrowth process competing for the point defects produced in the implant damage. Further confusing the results is the influence of the electrical activation of the implanted impurities that in turn may then substantially alter the point defect statistics. Some means of accounting for and ideally isolating the various processes are needed to make analysis manageable. Re-evaluation of the situation is appropriate, and work on this subject has been suspended for the moment.

C. Shallow Implanted Junctions

Initial work to characterize the physical issues crucial to the shallow implanted junctions necessary to very small geometry devices was begun. Thermally annealed, shallow phosphorus implanted layers, as well as thermally deposited and diffused layers of similar total charge, were fabricated. Both a single implant and tailored multiple implants to approximate a square profile for improved sheet resistance were employed. The implanted layers, particularly the tailored implanted layers, compared very favorably to the much deeper diffused layers in sheet resistance. Junction leakage currents were found to be improved considerable by backside argon implant damage gettering. These results are very promising, and emphasize again the potentially critical role of implanted layers and implant damage in small geometry device processing.

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CHEMICAL VAPOR DEPOSITION

K. C. Saraswat, T. I. Kamins, R. Reif, F. Mohammadi, and M. M. Mandurah

A. Polycrystalline Silicon

Arsenic doping of low pressure chemically vapor deposited (LPCVD) poly-silicon has been investigated. Both the film resistivity as a function of average dopant concentration and the microscopic location of the dopant atoms have been studied.

The films were deposited to a thickness of 0.5 µm at 620°C onto thermally oxidized silicon wafers. Arsenic ions were implanted with doses ranging form 1 x 10^{13} to 1 x 10^{16} ions/cm^2 at an evergy of 200 keV. For the average resistivity experiments the samples were coated with SiO_2 and then annealed for one hour at 1100°C to activate and uniformly distribute the dopant atoms.

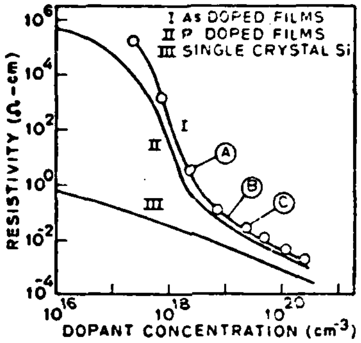

Fig. 2 Resistivity as a function of dopant concentration.

Fig. 2 shows the resistivity of the arsenic doped films as a function of average dopant concentration (implanted dose divided by film thickness) (curve I). The resistivity of phosphorus doped films (curve II), obtained in a previous study [1] and that of n-type single crystal silicon (curve III) are plotted on the same figure for comparison. At the lowest dopant concentration the poly-silicon films had a resistivity approximately five orders of magnitude higher than that of correspondingly doped single crystal silicon.

The resistivity decreased rapidly as the dopant concentration increased, finally falling to within half an order of magnitude of the single crystal resistivity at the highest dopant concentration. Throughout the whole range the arsenic doped films had higher resistivity than corresponding phosphorus doped films, as has been found for films deposited at atmospheric-pressure [2].

In the second part of the study, dopant segregation at the grain boundaries in poly-silicon was investigated. By observing the resistivity changes after various annealing cycles, information about the microscopic location of the dopant atoms could be inferred. All wafers were first annealed at 1000°C for one hour to activate and distribute the dopant and to stabilize the grain size so that further lower temperature annealing could not change the grain size appreciable [3]. In this way dopant segregation effects could be separated from those related to changes in grain size. After the initial 1000°C anneal, samples were then further annealed at 900, 850, and 800°C for 12, 24, and 64 hours respectively. These times were found to be adequate for all resistivity changes to reach saturation. Different samples were used for each of these three annealing temperatures.

Fig. 3 shows the room temperature resistivity as a function of annealing temperature for the three dopant concentrations corresponding to the points A, B, and C marked on Fig. 2. In all cases the resistivity increased from its initial 1000°C value on subsequent annealing, with a larger change caused by annealing at lower temperatures. The increase in resistivity was especially strong at the lowest dopant concentration, with approximately two orders of magnitude increase in resistivity after annealing at 800°C. This large change for the film corresponding to point A in Fig. 2 is consistent with the increasing importance of grain boundaries in lightly doped films.

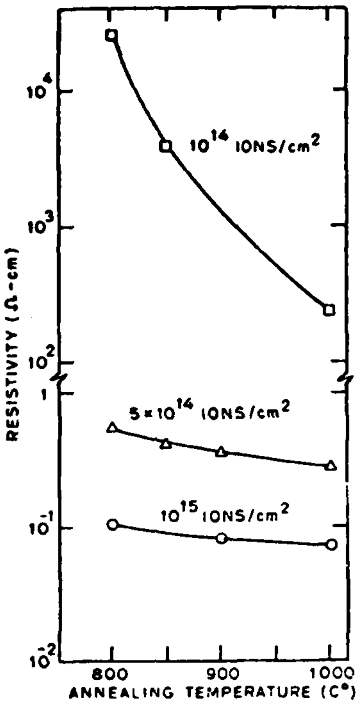

Fig. 3 Resistivity as a function of annealing temperature. The films annealed at 800, 850, and 900°C were preannealed at 1000°C.

The change in resistivity was reversible upon further annealing; i.e., by successively annealing the same sample at lower and higher temperatures, the resistivity would repeatedly increase and decrease, as shown in Fig. 4.

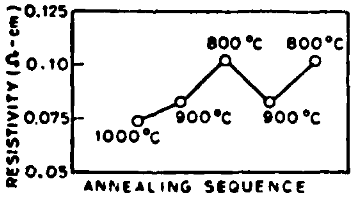

Fig. 4 Resistivity of a poly-Si film (implanted with 10^{15} ions/cm^2 arsenic) after successive annealing at different temperatures.

This reversibility is a definite indication of movement of dopant atoms between grains and grain boundaries, showing that the dopant atoms segregate to the grain boundaries at lower annealing temperatures. Such segregation is frequently observed in metals and alloys and has been previously suggested for poly-silicon [2,4]. Similar reversible changes were observed in phosphorus doped films, although longer annealing times were required to complete the segregation process.

The resistivities of the films were measured from 300 to 500°K. The logarithm of the resistivity was found to depend linearly on the reciprocal of the measuring temperature, indicating that the current transport is thermally activated. The activation evergies are summarized in Table 1. From the above measurements the proportion of atoms trapped at grain boundaries and the heat of segregation can be estimated.

Two models have been proposed to explain the resistivity as a function of dopant concentration in polycrystalline silicon. One model, proposed by Kamins [5] and developed by Seto [6], postulates that the dopant atoms are uniformly distributed throughout the material and that the conductivity is limited by carrier trapping at the grain boundaries. The second model, proposed by Cowher and Sedgwick [4], postulates that the conductivity is controlled by the segregation of the dopant atoms to the grain boundaries where they are trapped and become electrically inactive.

The first model (carrier trapping) has been more generally accepted because the second model (atom trapping) cannot explain the temperature dependence of the film resistivity. The present work suggests that the electrical condition in poly-silicon is influenced by both carrier and atomic trapping at the grain boundaries.

TABLE I

ACTIVATION ENERGY (eV)

DOSE ions/cm^2	ANNEALING TEMPERATURE (°C)			
	800	850	900	1000
1×10^{14}	0.465	0.386	--	0.279
5×10^{14}	0.0800	0.0746	0.0723	0.0719
1×10^{15}	0.0459	--	0.0459	0.0466

B. Epitaxy

Submicron silicon epitaxial films are becoming increasingly important with the development of VLSI technology. Not only will silicon epitaxy continue to be essential to bipolar technology, but it is also expected to expand into MOS technology [7]. For these applications, epitaxial layer thicknesses in the 0.5 - 1.5 μm range will be required.

The transients associated with the first few minutes of growth, however, impose severe limitations on the fabrication of such thin layers. During the initial stages of growth, both the silicon-deposition and the dopant-incorporation processes go through a transient, and several minutes are required before the steady-state epitaxial growth rate and doping level are established. In submicron films this transient time comprises a major fraction of the total deposition time, and the expected steady-state doping level may not be achieved.

This work deals primarily with the silicon-deposition process. The main objective of this work is to investigate the transients associated with the establishment of a steady-state silicon growth rate and their effect on the epitaxial doping level. The experiments described here concern the response of an epitaxial reactor to both increasing and decreasing changes in the gas-phase concentration of the silicon source.

All experiments were conducted in a horizontal rf-heated epitaxial reactor operating at atmospheric pressure. The corrected wafer surface temperature was approximately 1050°C. Hydrogen was used as the carrier gas, silane was the silicon source, and arsine diluted in hydrogen was the dopant source. The substrates were (100)-oriented silicon wafers with phosphorus dopant concentrations in the 10^{15} cm^{-3} range. The dopant profiles in the epitaxial layers were determined by capacitance-voltage measurements on planar p-n junctions and deep-depletion MOS structures [8]. Spreading resistance measurements were used to confirm the capacitance-voltage measurements.

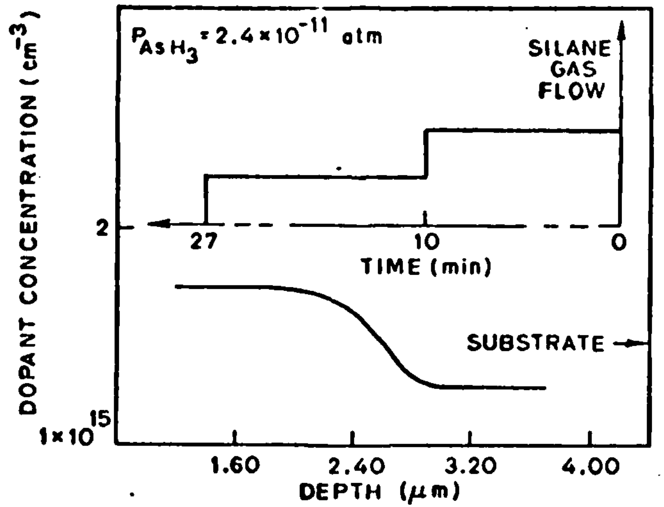

Fig. 5 Experimentally observed dopant concentration as a function of distance from the surface of the epitaxial film for the decreasing step change in silane gas flow indicated in the inset.

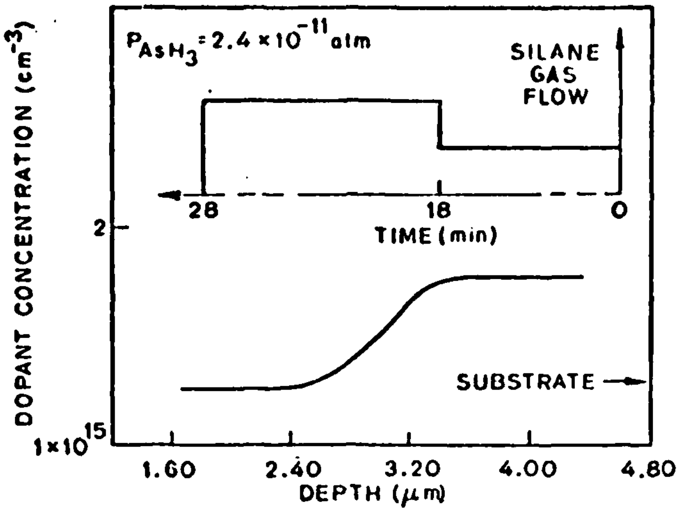

Fig. 6 Experimental dopant profile for an increasing step change in silane gas flow.

Figs. 5 and 6 show the measured dopant concentration as a function of distance from the surface of the epitaxial film for decreasing and increasing step changes in silane flow during deposition. The insets in the figures indicate the time-variation of silane flow during deposition for each case. At time t=0 (see Fig. 5) silane and arsine were introduced into the reactor tube to begin the deposition. The arsine flow was held constant throughout the entire deposition cycle which lasted 27 min. An arsine partial pressure of 2.4×10^{-11} atm was used to produce epitaxial doping levels in the 10^{15} cm^{-3} range. At t=10 min, the silane flow was abruptly lowered by decreasing the flow setting on the silane rotometer. The silane partial pressure was changed from approximately 9×10^{-4} to 4.5×10^{-4} atm, which produced epitaxial growth rates of about 0.34 and 0.17 μm/min, respectively.

The profiles in Figs. 5 and 6 show similar behavior. In both cases the transition occurs over a distance of approximately 1-1.2 μm, corresponding to several minutes of deposition. This similarity in the doping profile for increasing and decreasing silane gas flows suggests the importance of analogous physical mechanisms in the two cases. The information contained in the measured profiles is associated with the transient response of both the silicon-deposition process (since the growth rate changes) and and the dopant-incorporation process (since the doping level changes). The transient response of the dopant-incorporation process is fairly well understood [9]. Therefore, the transient associated with the silicon-deposition process can be obtained.

C. Silicides

1. Thermal Oxidation of WSi_2

As device dimensions continue to decrease due to the increasing level of integration, interconnection technology is becoming increasingly important. Highly doped poly-Si has been used widely for interconnections because of its high temperature process compatibility. However, the high resistivity and the large grains associated with doping and annealing of the poly-Si films impose restrictions upon circuit performance and fine pattern definition respectively. As an alternative to poly-Si, refractory metal silicides, such as $MoSi_2$ and WSi_2, are being proposed [10, 11] because of their high conductivity, small grain size, high temperature process compatibility and ability to be thermally oxidized to grow an insulating layer of SiO_2 on top of the film [12, 13]. In this work we have investigated growth kinetics of thermal oxidation of WSi_2 films sputtered on single crystal silicon and thermally oxidized silicon substrates.

Single crystal n-type Si wafers with (100) orientation and 5 to 10 ohm cm resistivity were used as substrates. On some of the wafers 100 nm SiO_2 was thermally grown. WSi_2 films were deposited on all samples by rf diode sputtering, in an argon ambient, from a hot pressed target of WSi_2. Since as deposited films were amorphous, annealing was performed at 1000°C, for 60 min., in N_2 ambient [14] to crystallize them. The annealed films were oxidized in dry O_2 and steam, at 1000, 1100 and 1200°C, for up to 30 min. The composition of the oxidized films was examined by X-ray diffractometry. Surface roughness and oxide thickness were measured by a taly step.

The films oxidized in dry O_2 always had a very rough surface with a yellow powder present. This powder was identified to be WO_3 by X-ray diffraction. Similar formation of MoO_3 upon dry oxidation of $MoSi_2$ has also been reported [15]. Formation of WO_3 can seriously degrade the properties of the oxide as well as silicide films. In order to prevent formation of WO_3, wet oxidation of WSi_2 films was performed. Nitrogen was bubbled through heated water to obtain steam for oxidation. The oxidized films had very smooth surfaces, and no WO_3 could be detected. The result of X-ray diffractometry also showed that as oxidation proceeds WSi_2 reacts with H_2O to form SiO_2 and W_5Si_3. The mechanism of conversion of WSi_2 to W_5Si_3 is different for two types of substrate. The result of oxide thickness measurement for the two different substrates has been plotted in Fig. 7. It can be seen that the oxidation of WSi_2 films without a source of free Si atoms underneath has much lower dependence upon oxidation temperature. From this study activation energy of SiO_2 growth was determined to be 23 Kcal/mole for WSi_2/Si films and 8-9 Kcal/mole for $WSi_2/SiO_2/Si$ films.

2. WSi_2 Gate MOS Capacitors

It has been shown that for a few thousand Å thick films of WSi_2, obtained by vacuum evaporation techniques, the resistivity is on the order of 10^{-4} Ωcm [11,16]. Chemical reagents commonly used for cleaning silicon do not have any reaction with WSi_2, wnereas the chemicals used for etching

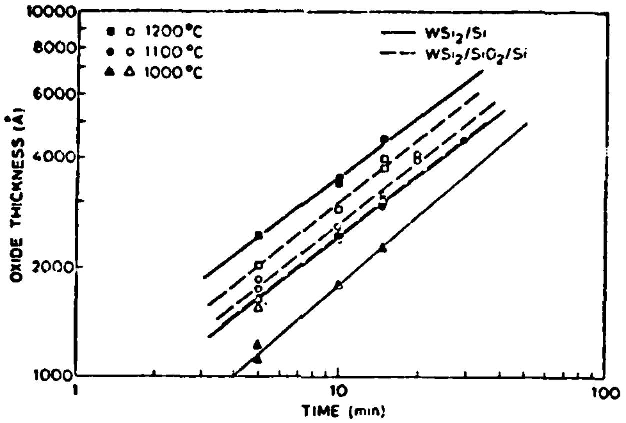

Fig. 7 Thickness of SiO_2 grown as a function of growth time.

silicon also etch WSi_2 [16]. Thermal oxidation of WSi_2 has been performed to grow SiO_2 of good quality [13, 17]. Although the as deposited films of WSi_2 have very small grains, prolonged high temperature annealing increases their size substantially. However, the maximum grain size still remains lower than 1000 Å [16]; therefore, it must be possible to define very fine lines in thin films of WSi_2. Thus it is evident that WSi_2 is highly suitable to form gate and interconnections in MOS ICs and its use should substantially improve their performance. In this work, fabrication and characterization of WSi_2 gate MOS devices are presented.

Single crystal n-type silicon wafers, with (100) orientation and 2-4 Ωcm resistivity, were used as substrates to fabricate MOS capacitors with gate oxide thickness ranging from 600 to 4000 Å. Different oxidation times were used at 1000°C in steam to obtain different oxide thicknesses. Following the oxidation all of the wafers were annealed together in N_2 at 1000°C for 30 minutes to ensure the same value of Q_{ss}. A 2500 Å thick layer of WSi_2 was deposited on all samples using rf diode sputtering in argon atmosphere.

The substrate temperature was kept below 300°C and the rate of deposition was 360 Å/minute, with a peak voltage of 1.5 keV and an rf power of 280 watts. The target was made of hot pressed WSi_2. Photolithography was performed to define the gates. A 2% NH_4F + 98% HNO_3 solution was used to etch WSi_2. The as deposited WSi_2 was amorphous, therefore a 1000°C anneal in argon was performed for one hour to make the films polycrystalline [16]. This anneal reduced the resistivity of WSi_2 from 6×10^{-4} to 10^{-4} Ωcm and also annealed any surface damage encountered during sputtering. A 1.5 μm thick layer of aluminum was deposited on the backside to obtain good ohmic contact. Finally, the wafers were annealed in forming gas (10% H_2 + 90% N_2) at 450°C for one hour.

C-V measurements were performed on the capacitors at a frequency of 1 MHz. From these measurements the gate oxide thickness, W_{OX}, flat-band voltage, V_{FB}, and threshold voltage, V_T, were estimated. W_{OX} was also independently measured by ellipsometry prior to WSi_2 deposition. Fig. 8 shows a plot of V_{FB} and V_T as a function of W_{OX}. From these curves the value of work functions ϕ_m and Q_{ss} can be determined.

Under thermal equilibrium, the flat-band voltage of a MOS structure fabricated on an n-type substrate can be expressed as follows [18]:

$$V_{FB} = \phi_{ms} + \frac{Q_{OX} W_{OX}}{\varepsilon_{OX}} \qquad (1)$$

Where Q_{OX} is the total oxide charge density, ε_{OX} is the permittivity of SiO_2 (3.4×10^{-13} F/cm), and ϕ_{ms} is the metal-to-silicon work function given by the relation [18]:

$$\phi_{ms} = \phi_m - X + \frac{E_g}{2} - \Psi_n \qquad (2)$$

where ϕm is the metal work function, X is the semiconductor electron affinity, E_g is the band gap, and Ψ_n is the magnitude of the bulk potential of Si.

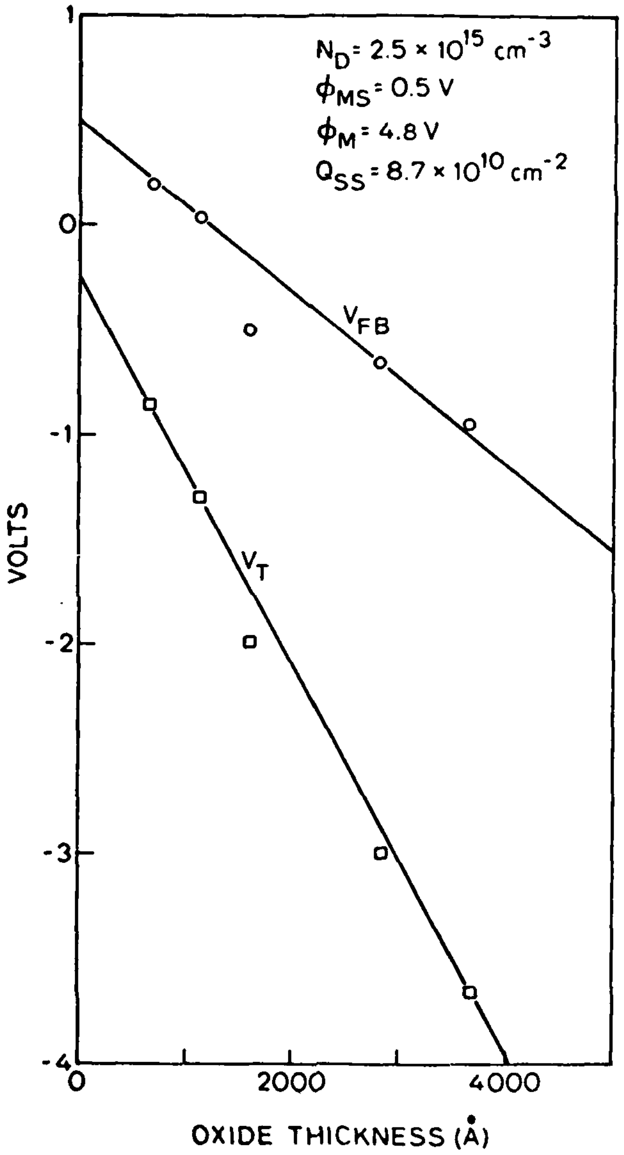

Fig. 8 V_{FB} and V_T as a function of gate oxide thickness.

From Eq. (1) it is evident that the slope of V_{FB} vs. W_{OX} curve will give the total oxide charge density and intercept at zero oxide thickness will give the value of ϕ_{ms}. Using Eq. (2), ϕ_m can be caluclated since the value of X and E_g are known and Ψ_n can be calculated if the substrate doping density is known.

As shown in Fig. 8, excellent linearity was obtained in the plot of V_{FB} vs. W_{OX}, indicating the validity of the C-V method to obtain ϕ_m and Q_{OX}. Bias-stress C-V measurements showed presence of negligible mobile charge contamination and thus it can be assumed that $Q_{OX} = Q_{ss}$ (the density of fixed interface charge). From Fig. 8 the value of Q_{ss} is thus 8.7×10^{10} charges/cm^2. From the intercept of V_{FB} vs. W_{OX} curve the value of ϕ_{ms} is 0.5 eV. From C-V plots the value of doping density was found to be about 2.5×10^{15} corresponding to $\Psi_n = 0.31$ eV. With X and E_g taken 4.05 eV and 1.12 eV respectively [18], the value of the metal work function of WSi_2 was estimated to be 4.8 eV.

High frequency and quasi-static C-V measurements [19] were performed on the capacitors with 1100 Å gate oxide thickness and surface state density distribution (N_{st}) in the band gap was calculated. Fig. 9 shows the results of 1 MHz and quasi-static C-V measurements. Fig. 10 plots N_{st} in the band gap calculated from the two C-V measurements. The value of N_{st} near the mid-band was about 2×10^{10} cm^{-2} eV^{-1}.

The values of Q_{ss} and N_{st} are quite comparable to that of Al-gate or Si-gate MOS structures. The work function of WSi_2 is slightly higher than Al or Si. With accurate knowledge of the work function, the fabrication process can be designed accordingly to obtain proper threshold voltages of the MOS devices.

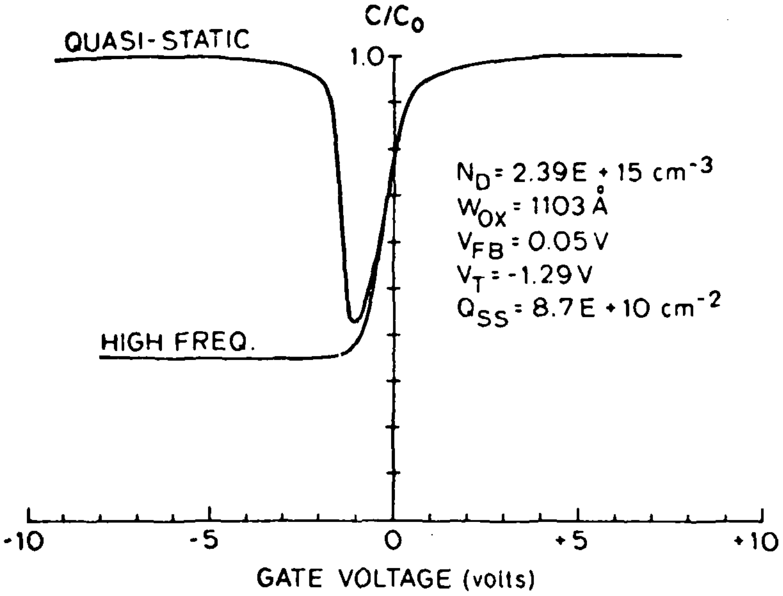

Fig. 9 Quasi-static and high frequency C-V measurements.

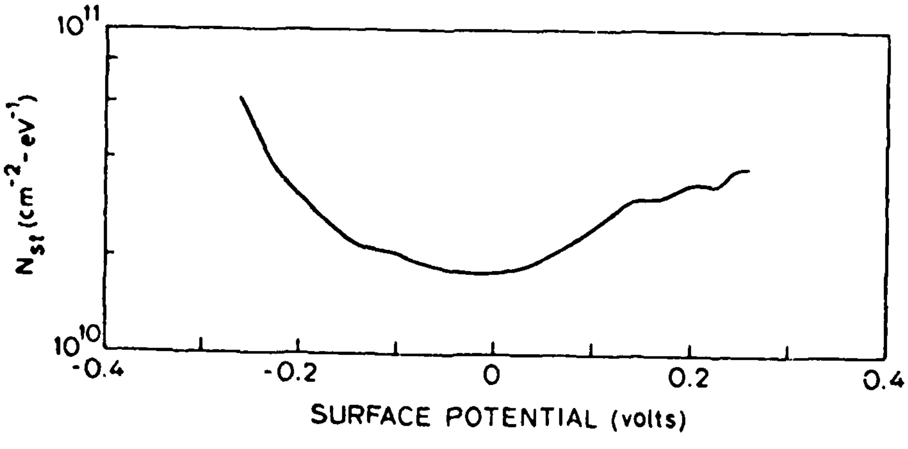

Fig. 10 Surface state density in the band gap.

WSi_2 appears to be highly attractive as an alternative to polycrystalline silicon to form gate and interconnections in MOS integrated circuits. Because of its low resistivity the resistance of the interconnecting lines should reduce markedly. The material appears to completely compatible with the current fabrication processes. MOS devices fabricated with WSi_2 as the gate material exhibit excellent SiO_2-Si interface properties, i.e. low Q_{ss} and N_{st}. The value of the work function of ϕ_m is slightly higher than that of Al or Si. The process must be modified slightly to obtain circuit compatible threshold voltages of the MOS transistors.

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MATERIALS ANALYSIS AND INTERFACE PHYSICS

C. R. Helms, S. A. Schwarz, R. W. Barton, J. Rouse

In this period much of our activity has centered on determining what factors affect sensitivity, depth resolution, quantitative analyses, etc., for Auger sputter profiling, photoelectron spectroscopy and secondary ion mass spectrometry so that the proper technique can be applied to the proper problem and each technique can be implemented to its full potential. In addition to studies of the capabilities and limitations of the above-mentioned microanalytical techniques, we have used these capabilities for critical measurements of interface properties in conjunction with other groups in the program. A summary of our major accomplishments in this part of the program are described below.

A. Sensitivity and Spatial Resolution of Auger Electron Spectroscopy

In general sensitivity in AES is determined by the signal-to-noise ratio which is given by:

$$\frac{S}{N} = A\sqrt{It}\left(\frac{\Delta E}{E}\right)^{1/2} V_{ptp}$$

where A is a constant, I is the beam current, ($\Delta E/E$) is the resolution of the analyzer, t is time, and V_{ptp} is the modulation voltage. We will define the maximum AES sensitivity as the concentration of the element with the strongest Auger transition for which S/N = 1.

From extrapolating data taken at much less ideal conditions, a value of maximum sensitivity of AES of $\sim 10^{17}$ cm^{-3} can be estimated. This value of maximum sensitivity, however, does not correspond to all elements but to the maximum-strength AES transitions such as the Ag MNN transition or the Cl LMM transition. Maximum sensitivities for other elements of interest are listed in Table 2 within ± half order of magnitude. These values are based on the assumption that there are no interference effects from neighboring transitions.

To obtain these sensitivities within a 30-min data collection time, a 100 μA beam current would be required. Presently, typical guns with LaB_6 emitters can provide this beam current with a minimum spot size about 10 μm in diameter. This corresponds to a current density of 100 A/cm^2, a power density of 5×10^5 W/cm^2, and a total power dissipation of ~1/2 W. These levels are sufficient to cause local melting of silicon under typical conditions. To bring beam effects to acceptable levels under these conditions, rastering the electron beam over a 100 x 100 to 200 x 200 μm area is required. In Fig. 11 the variation of maximum sensitivity of AES as a function of beam diameter is presented. The solid curve is for Si; the two dashed curves

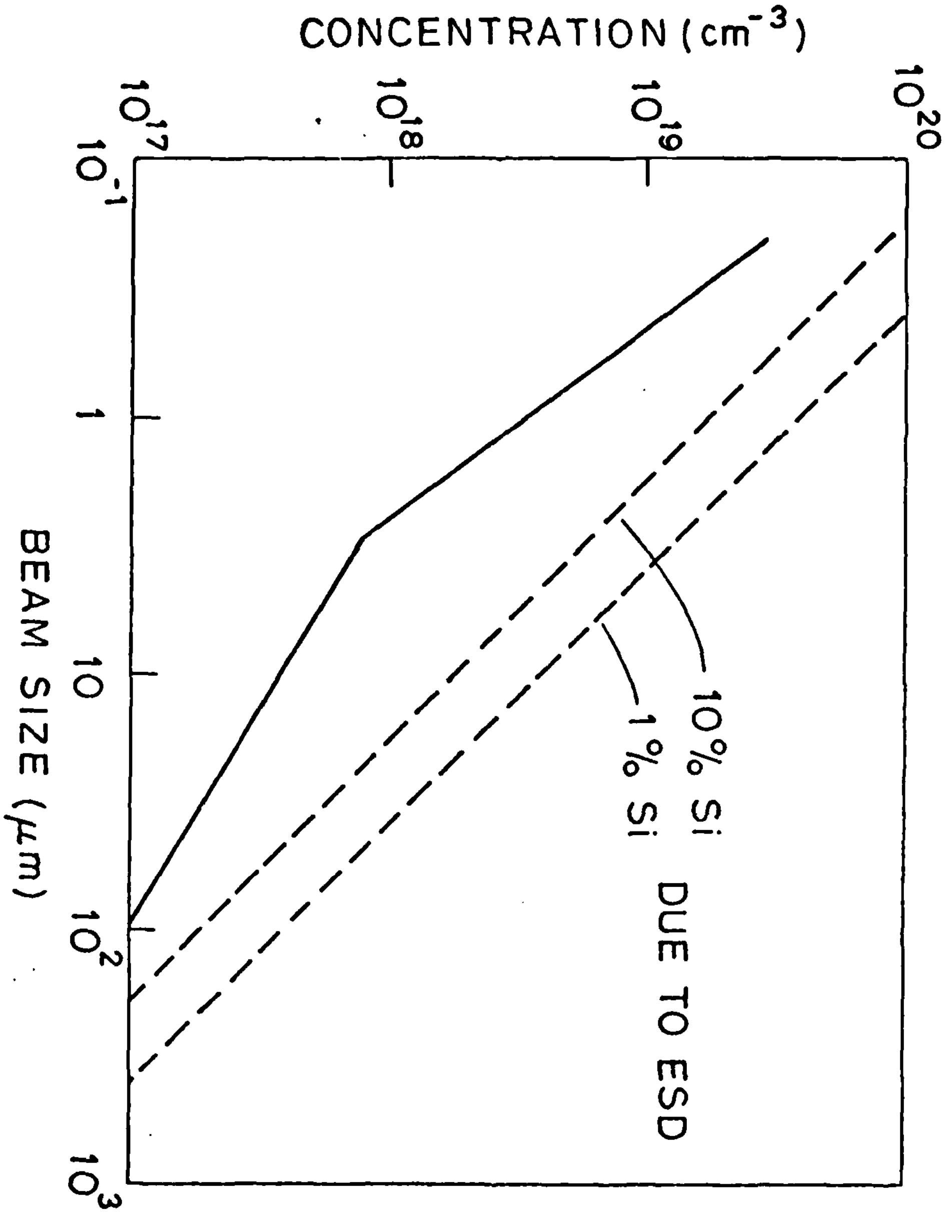

Fig. 11 Maximum Sensitivity of AES (to chlorine or silver transitions) as a function of electron beam diameter Dashed curve corresponds to the degradation in sensitivity in SiO_2 due to electron stimulated desorption (esd). The 10% Si and 1% curves correspond to beam size and sensitivity such that the spectra will contain 10% or 1% contribution from elemental silicon due to esd.

Table 2

MAXIMUM ESTIMATED AES SENSITIVITIES

Element	Sensitivity	Comments
B	10^{18} cm^{-3}	Ar interference
C	3 x 10^{17} cm^{-3}	background contamination
N	3 x 10^{17} cm^{-3}	---
O	3 x 10^{17} cm^{-3}	background contamination
F	3 x 10^{17} cm^{-3}	---
Na	10^{18} cm^{-3}	beam induced drift
Al	3 x 10^{17} cm^{-3}	Si interference
Si	3 x 10^{17} cm^{-3}	---
P	3 x 10^{17} cm^{-3}	Si interference
Cl	10^{17} cm^{-3}	Ar interference
As	3 x 10^{18} cm^{-3}	---
Sb	10^{17} cm^{-3}	---

represent the limit in SiO_2 for beam energies of 4.5 keV with the indicated amounts of elemental silicon present in the spectrum due to electron stimulated desorption.

B. An Ion Knock-On Mixing Model

Depth profiles obtained from ASP or SIMS experiments are broadened by ion beam-induced atomic mixing [1, 2, 3]. In this period, we developed a model for ion knock-on mixing [4] based on analogy-to-thermal diffusion theory. The model leads to a simple relationship which predicts the broadening observed in a sputter profiling experiment. We have shown that the broadening of the Si/SiO_2 interface for low energy Ne^+, Ar^+, and Xe^+ bombardment is consistent with the mixing model.

The ion knock-on mixing model [4, 5] developed is based on an analogy to thermal diffusion theory. A similar approach has been taken by Haff and Switkowski [3]. In their paper, an effective diffusion coefficient D is derived in terms of various parameters including a cascade radius and the stopping power of the ion. A diffusion time t must be inferred in order to determine the broadening observed in a sputter profiling experiment. In our model, an effective broadening parameter $W^2 = Dt$ is derived and expressed in terms of the sputtering yeild S, a measurable quantity. The stopping power effect in Haff's model is inherent in the sputtering yield.

Our derivation is based on the assumption that an atom in the bombarded solid undergoes a number of random collisions N and is detected immediately prior to or after its escape from the surface. In an ASP experiment, this assumption is valid if the escape depth L is small (~5 Å) or is much less than the ion broadening parameter W.

We have performed ASP experiments [4] to examine the broadening of the Si/SiO_2 interface as a function of ion energy for Ne^+ and Xe^+ bombardment. The measured interface widths are plotted in Fig. 12. The solid curves are calculated form the mixing model with an assumed original 10% to 90% interface width of 3.6 W_0 = 2.0 nm and with $(\overline{a^2})^{1/2} = a_{rms} = 0.33$ nm. The divergence of the solid curves from the data at high energies is due to the increase of a_{rms} with energy. The dashed curves are a higher energy approximation which we discuss in the next section. If the value of 3.6 W_0 is increased beyond 2.0 nm, the curves in Fig. 12 will move closer together. Thus, at a particular ion energy, the different broadening parameters obtainaed for Ne^+, Ar^+, and Xe^+ provide good evidence for the actual interface width.

C. Redistribution of Phosphorus During the Thermal Oxidation of Silicon

During the thermal oxidation of heavily phosphorus-doped silicon, phosphorus, which is relatively insoluble in SiO_2, is rejected by the oxide and pushed into the silicon where it diffuses away from the interface. This process was first described in detail by Grove et al [6]. If oxide growth and diffusive transport are the only operative mechanisms in the process, the phosphorus concentration near the Si/SiO_2 interface should be no more than twice the bulk concentration for typical conditions, as illustrated in Fig. 13. However, a magnified view of the interfacial region obtained using Auger sputter profiling shows an anomalous buildup of phosphorus near the interface, as illustrated in the inset in Fig. 13. This phosphorus pileup has been observed by several groups [7-11]. An explanation of its mechanism was the goal of this part of the program.

In order to determine the mechanism for the phosphorus pileup, we have determined the dependence of the observed phosphorus distribution

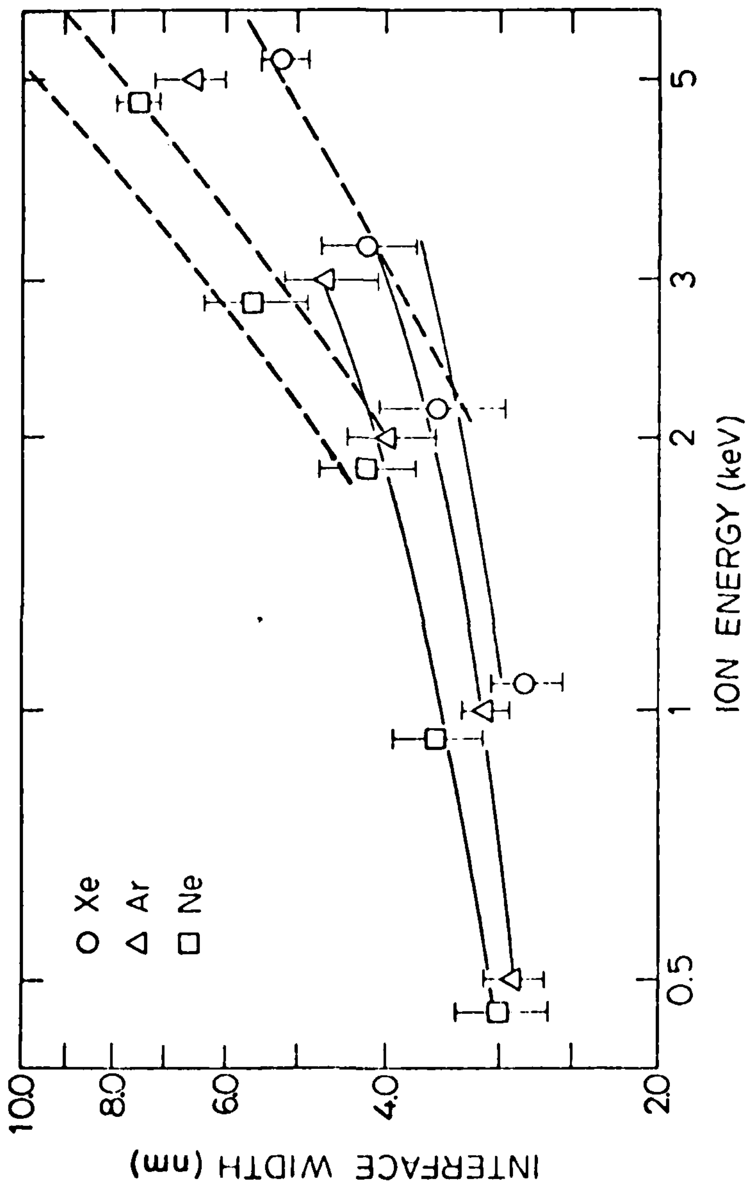

Fig. 12 Average and standard deviation of the measured 10-90% Si-SiO$_2$ interfaced widths as a function of ion energy for Ne$^+$, Ar$^+$, and Xe$^+$ bombardment. Solid curves are the low energy predictions of our mixing model for an original interface width of 20 Å. Dashed curves are predicted by a high energy extension of the model.

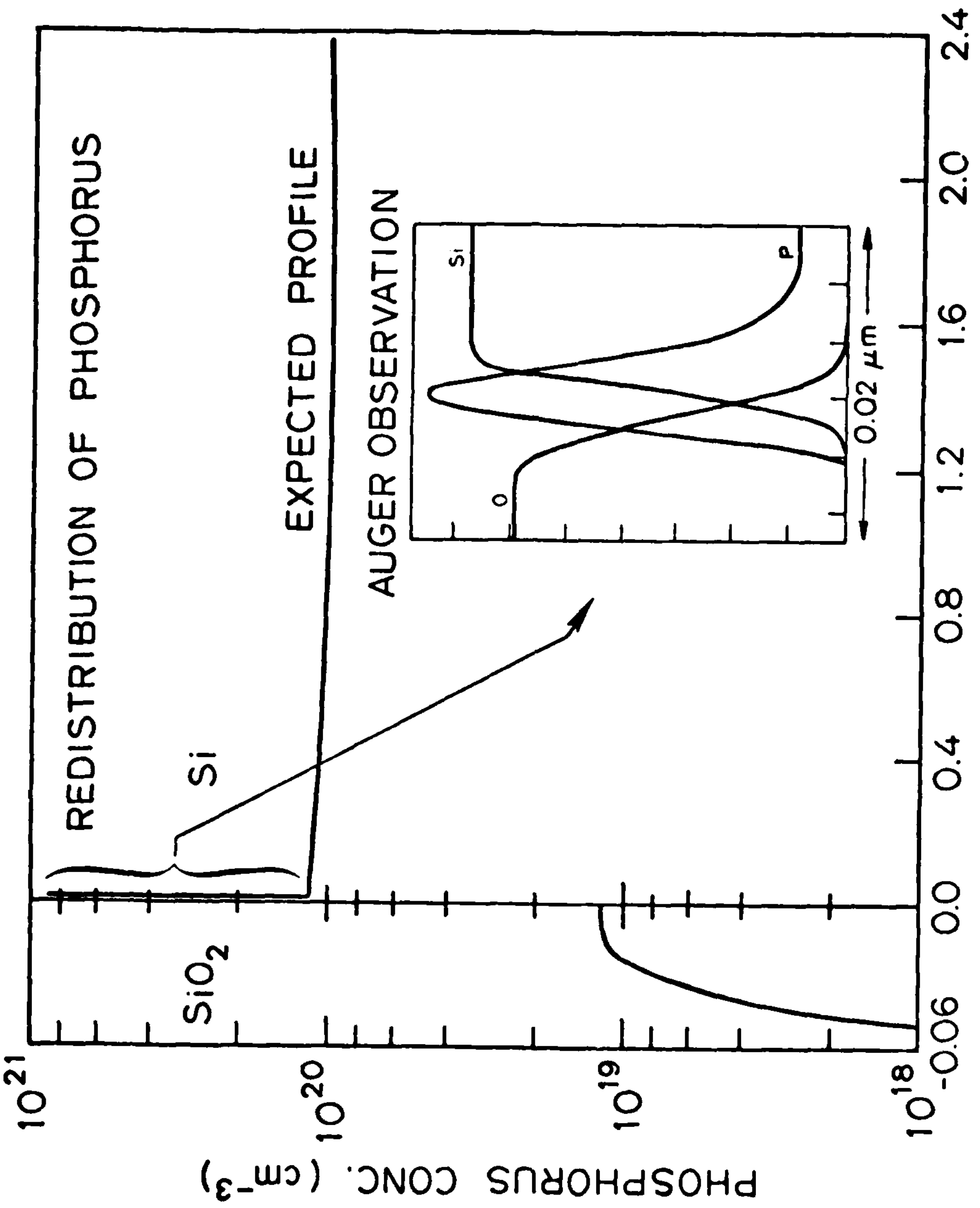

Fig. 13 Illustration of the phosphorus pileup effect at the Si-SiO$_2$ interface for a bulk concentration of 10^{20} cm^{2} and a sample oxidized at 1150°C for 10 min. Except for the delta-function-like contribution near the interface, the profile shown has been calculated using traditional diffusion redistribution theory. Note, the falloff in phosphorus concentration at the surface of the oxide is due to evaporation of phosphorus. The insert shows an actual measurement from this work of the near interface region, indicating the anomalous pileup observed.

on several different processing conditions. We have measured the dependence of the phosphorus distribution on the time of oxidation. We have also determined the effect of post-oxidation anneals. And, finally, we have investigated the effect of an additional electrically compensating dopant: boron.

As has been pointed out previously, the measured phosphorus profiles are not consistent with a simple diffusion-redistribution model, as these models would predict a much smaller peak concentration with the pileup region extending much further into the silicon.

Our data can only be explained by considering the interface as a sink for phosphorus either during oxidation or during anneals. This behavior is therefore a property of the interface and not a direct consequence of the oxidation process itself. The behavior of the Si/SiO_2 interface as a sink for phosphorus implies that the chemical potential for phosphorus has a sharp minimum at the interface.

There are several mechanisms which can account for this chemical potential sink at the interface. Since the phosphorus is positively charged in the silicon, it might be attracted to a negative electrical potential at the interface. Since the phosphorus is a different size than silicon and will have, in general, a different bonding geometry, it might reduce the interfacial strain energy. The phosphorus might also form a chemical species at the interface (an SiP or an SiP_xO_y) which is not observable in the bulk. And finally, the phosphorus might accumulate where vacancies, with which it is normally paired, have been depleted.

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COMPLETE PROCESS AND DEVICE SIMULATION

R. W. Dutton, N. Chan, D. D'Avanzo, E. Demoulin, H. G. Lee, S. Y. Oh,
D. Estreich, S. Hansen, C. Price, and D. Ward

The overall goals of the Complete Process and Device Simulation activity include:

1) Model implementation and upgrading of the SUPREM program
2) Development of device analysis to couple directly with SUPREM
3) Test structure and other experimental work to validate the process and device models
4) Dissemination of the results to industry.

The results and discussion below focus primarily on the last three items since previous sections have outlined SUPREM-related activities.

During this contract period the following highlight accomplishments were achieved:

1) The two-dimensional Poisson solution program TANDEM was developed and tested on TI devices. Results show excellent agreement with both experiment and 2D solutions including one carrier in addition to Poisson.

2) A totally new quasi-2D MOS device analysis method has been developed and demonstrated for the dc case. The method is more than an order-of-magnitude faster than conventional methods and it may be possible to apply the method to transient device analysis.

3) Device analysis and test structure evaluation of DMOS devices have been completed. The results show that in the range of 2 μm effective channel length, velocity saturation controls electrical performance and further scaling-down of DMOS gives no benefits concerning current handling and switching speeds.

4) The CMOS latch-up studies were completed including a careful investigation of scaled-down devices. Several factors such as contact resistance and lower supply voltages tend to decrease latch-up susceptibility.

5) Experimental characterization of MOS device capacitance has confirmed the earlier prediction of the non-reciprocal gate capacitance effects. These results represent a major breakthrough.

6) The test structure methodology for lateral profile measurements has been extended using new analytical tools. A two-dimensional process modeling capability has been coupled with TANDEM to

analyze and extract profile information near locally oxidized regions. In addition, the profile measurement method has been tested on DMOS structures.

7) A high frequency bipolar transistor CAD model was developed via two-dimensional device analysis. This model includes both dc and ac effects associated with emitter sidewall charge storage.

8) The annual review was held on July 9, 1979 and the results of the overall program were presented and discussed to the industry. The attached program and attendance sheets give an overview of participation.

In the following few subsections the accomplishments are reviewed further.

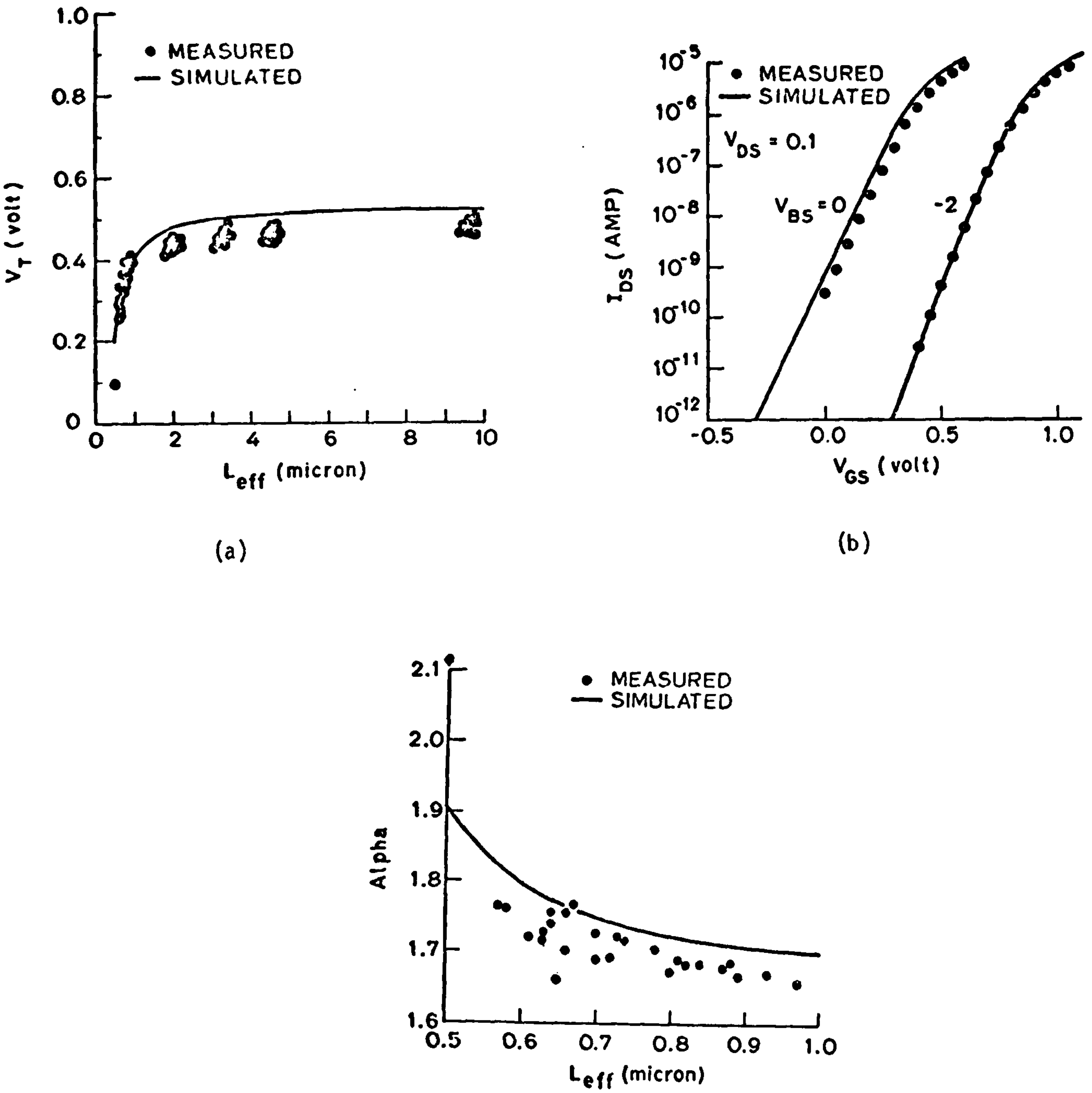
An extensive set of analyses capabilities for VLSI devices based solely on 2D Poisson solutions have been demonstrated. This latter work couples directly with the TI contract. At present it appears to be feasible to compute subthreshold, punchthrough, threshold and back gate bias using only the TANDEM Poisson solutions. The characterization of TI devices includes an extensive set of statistical parameters. Both subthreshold and above-threshold data on 141 devices have been measured. Preliminary results of 2D Poisson analysis indicates that observed variations with channel length are a direct consequence of ΔL variations for the measured impurity profiles and gate oxide thickness. Typical data and simulated results are shown in Figure 14.

During this period substantial progress was made in addressing two-dimensional analysis and in particular grid constraints. A study of restrictions for MOSFET devices based on geometry of both inversion layer and source-drain diffusions showed that an irregular non-rectangular grid can give as much as a 20:1 advantage in effective utilization of the mesh. A novel dc analysis method which maps a Poisson solution into a boundary value problem has been demonstrated. Using the boundary value solution for charge and a one-dimensional carrier transport along the surface, less than 5% error in current between the new method and CADDET has been shown over the voltage range of $0 < V_{DS} < 4$ V (see Figure 15). The boundary value method uses 40 times fewer grid points and converges to 10^{-6} V whereas CADDET uses a 10^{-3} V convergence criteria.

A highlight activity for this period is the characterization -- both experimentally and using CADDET analysis -- of the non-reciprocal MOS gate capacitance effects. Experiments clearly show the effects predicted (see Fig. 16) and reported in the IEEE JSSC article, October 1978. Similar results were obtained with CADDET and presently an analytical form to model the inversion charge effects is being formulated.

Analytical models for two-dimensional ion implantation, diffusion and oxidation including local oxidation have been implemented in a general purpose program. An experiment with both a local oxidation mask edge (case B) and uniform oxidation (case A) over the boron implanted regions was used to test the model. Results shown in Fig. 17 indicate that over a substantial range of process temperatures the model predicts the lateral diffusion quite accurately. For the experiment, the final oxide thickness grown was the same for all process temperature.

The third annual Process Modeling one-day short course was held on July 9, 1979. Attendance was 187 including participants from most major IC and systems contractors (see attached list). Discussions during the meeting clearly indicate that SUPREM II is the preeminent process modeling program. Participants were extremely interested in having the process models quickly incorporated into SUPREM.



(a)

(b)

(c)

Fig. 14. Characterization of short channel MOSFET's (a) V_T vs. L_{eff} for 141 devices and 2D simulation results. (b) Typical subthreshold plot and simulation of log I_{DS} vs. V_{GS} at V_{SB} = 0 and V_{SB} = 2 V. (c) The variation of the exponential non-ideality factor both measured and simulated as in (b).

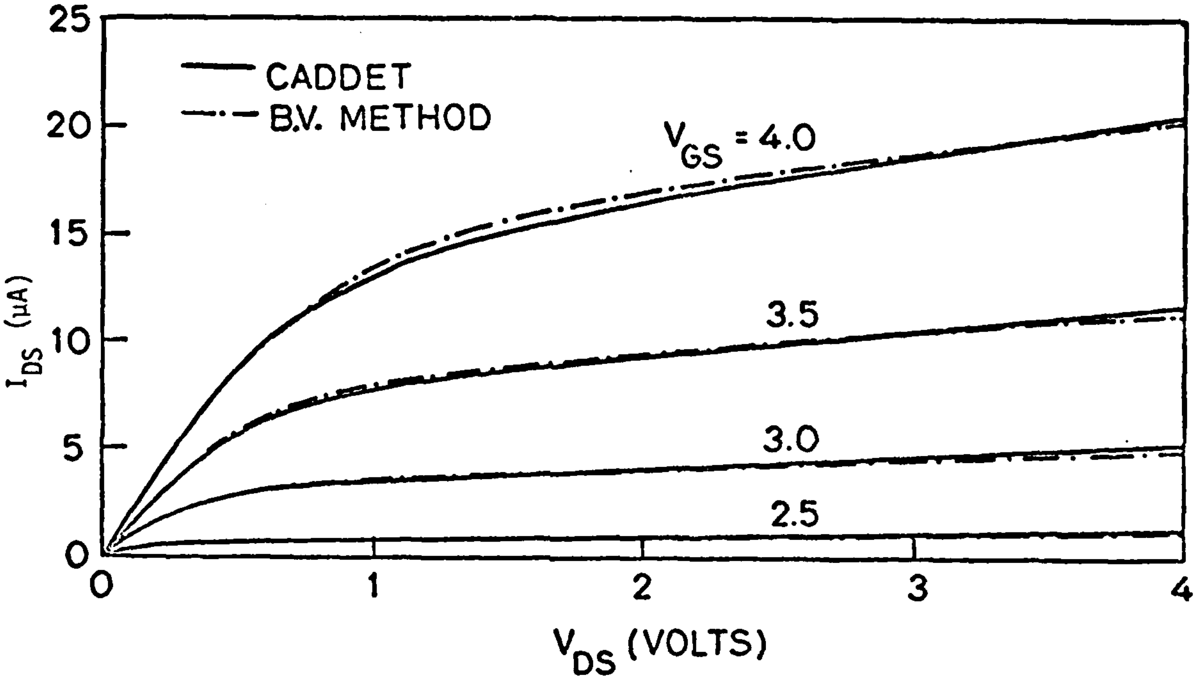


Fig. 15 Comparison of 2D device simulations of I_D vs. V_{DS} using CADDET with 1840 grid points and the new boundary value method with 46 grid points.

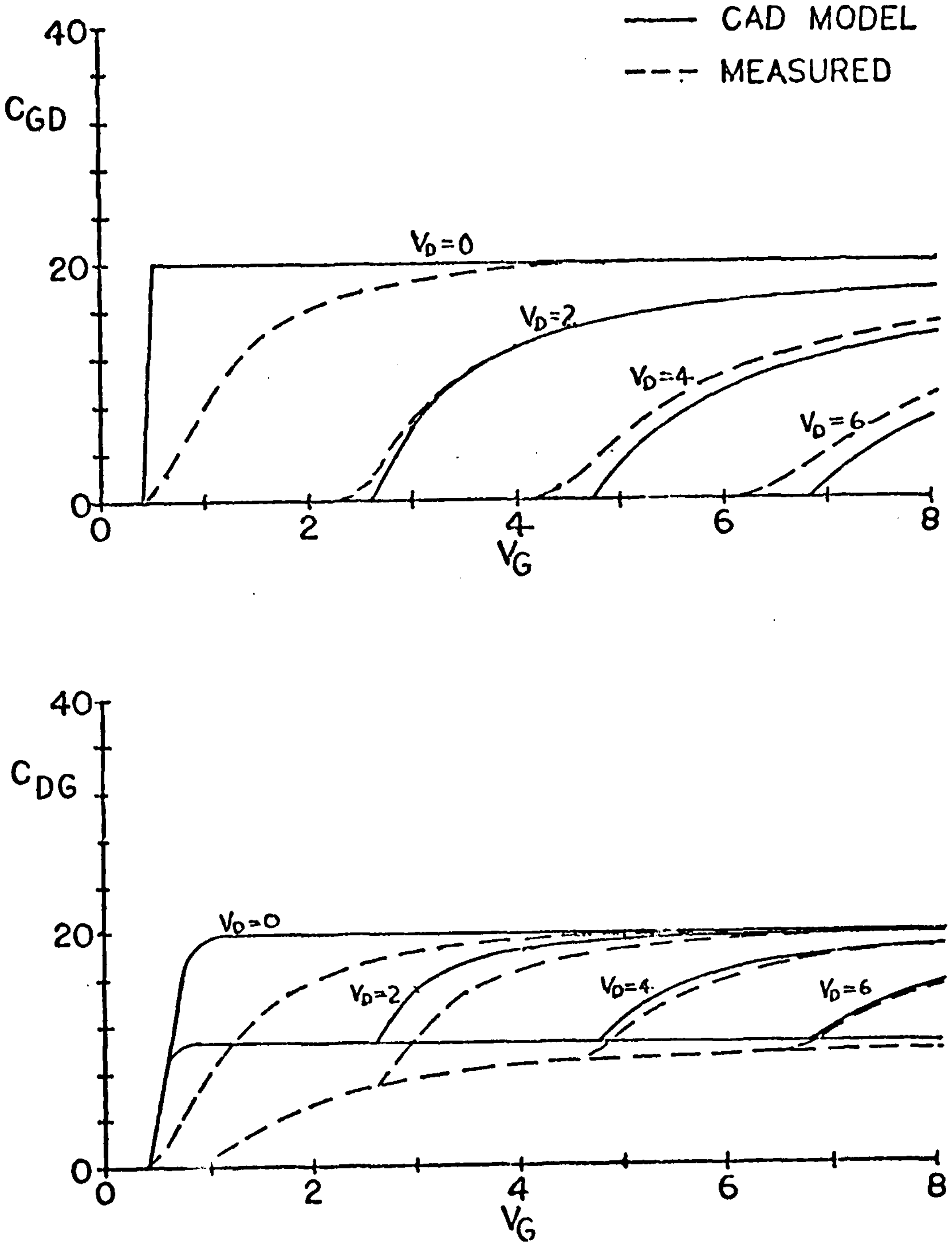


Fig.16 Theoretical and measured gate-drain capacitances.

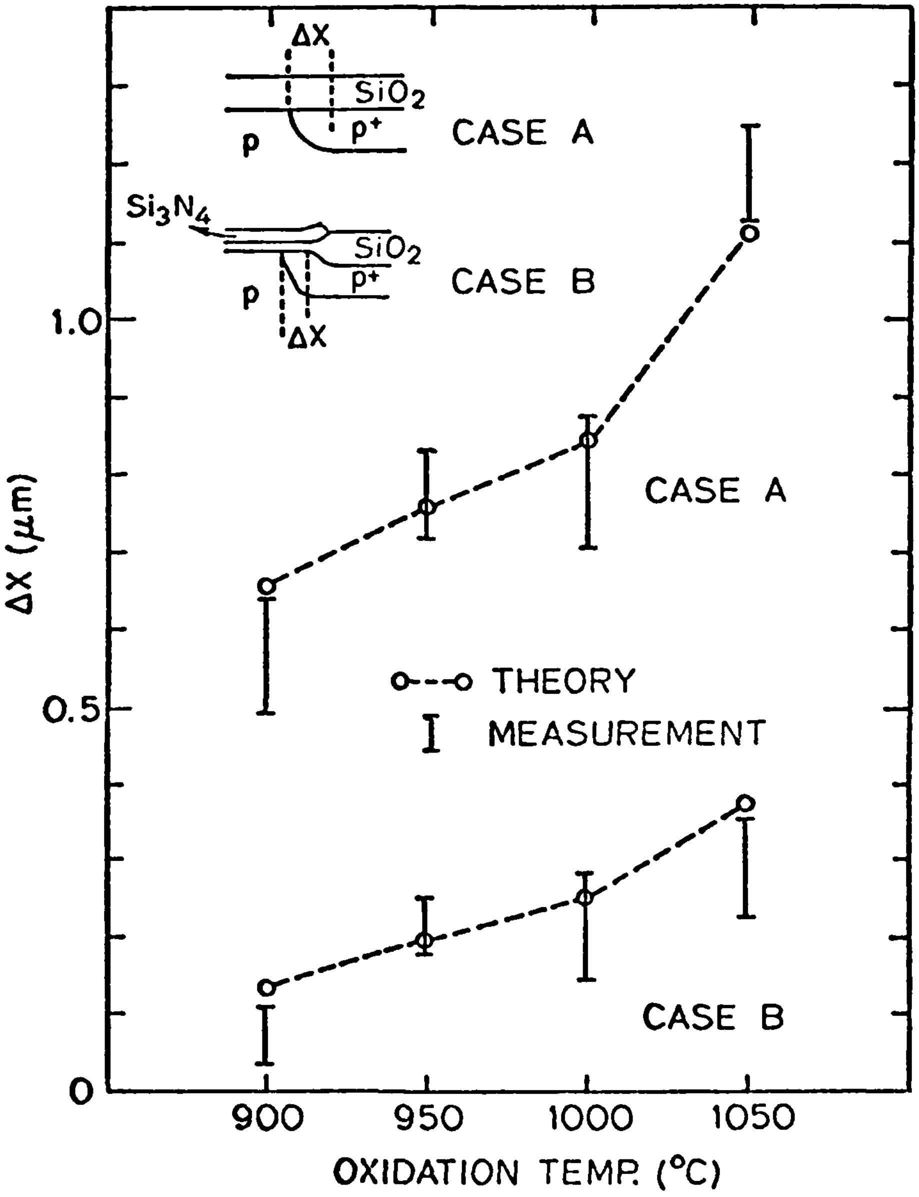


Fig. 17 Measured and simulated results of lateral diffusion of boron for both uniform thick field and locally oxidized surfaces.

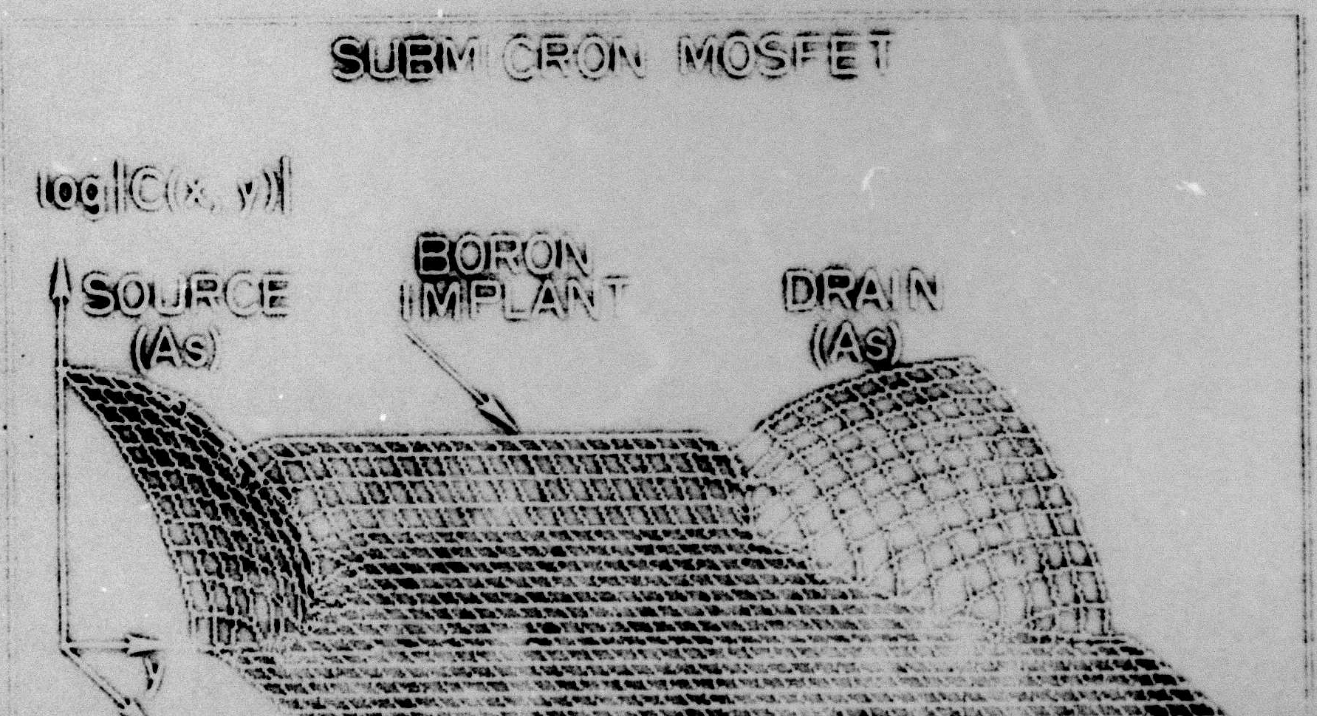
Continuing Education in Engineering
University Extension, and the College of
Engineering, University of California,
Berkeley, in cooperation with the Electrical
Engineering Department, Stanford University

announce a one-day program

Computer Aids for IC Technology and Device Design

July 9, 1979

Stanford, California



Computer Aids for IC Technology and Device Design

a one-day program
Monday, July 9, 1979
Stanford, California

Process and device modeling for IC technologies are areas that will become of increasing importance for VLSI. As devices are scaled down, the interaction of impurity profiles and surface geometries becomes tightly coupled. This one-day program reviews the state-of-the-art in process and device modeling. New aspects appropriate to VLSI are emphasized, such as thin oxides, low pressure CVD, laser and e-beam annealing, oxidation enhanced diffusion, bulk defect generation, and interface charge and annealing.

The format for the program consists of lectures discussing current problems in IC processing and research efforts at Stanford. Background material is provided, based on chapters written by the instructional staff which will be part of a text, *Integrated Circuit Process Models*, edited by James D. Meindl.

One important and novel aspect of this one-day program is to provide IC technologists with an update on advances in process modeling. In addition, the Stanford process simulation program SUPREM provides a portable means to carry this knowledge into IC engineering practice. The conclusion of the course focuses on an update concerning SUPREM as well as discussions of device analysis based on SUPREM.

Location: Terman Auditorium, Stanford University, Stanford, California

Fee: $125 (includes lecture notes and luncheon). Enrollment is limited, and advance enrollment is required.

Program Organizer
ROBERT W. DUTTON, Associate Professor of Electrical Engineering, Stanford University

Faculty Adviser
RICHARD S. MULLER, Professor of Electrical Engineering and Computer Sciences, University of California, Berkeley

University Extension Coordinators
HELEN BARRY and LINDA REID, Continuing Education in Engineering, University Extension, University of California, Berkeley

Program

7:45-8 a.m.	Registration	
8-8:20	Introduction	Meindl
8:20-9:10	Patterning	Pease
9:10-10	Implantation and Annealing	Gibbons
10-10:20	Coffee break	
10:20-11	CVD of Epitaxial Si	Reif
11-11:40	Polycrystalline CVD	Kamins
11:40-12:20 p.m.	Refractory Metal Silicides for VLSI Applications	Saraswat
12:20-1:15	Lunch	
1:15-2	Oxidation Kinetics	Plummer
2-2:40	Diffusion and Defects	Lin
2:40-3	Coffee break	
3-3:30	Interface Charges	Deal/Razouk
3:30-3:50	Interface Analysis	Helms
3:50-4:20	Material Science Perspective	Tiller
4:20-4:50	SUPREM II	Dutton
4:50-5:20	Device Analysis	Dutton

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